Sepideh Asadi

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SUMMARY

Final year PhD student in computer science. Background in Software Verification and Formal Methods. Research experience in automated symbolic model-checking, incremental verification of large-scale programs, and SAT/SMT solving. Highly motivated to integrate formal verification into software development process. During my PhD studies I have contributed to two projects:

UpProver An SMT-based bounded model-checker for incrementally verifying changes in program revisions
HiFrog A function-summarization-based BMC based on OpenSMT solver for verifying C programs

EDUCATION

Ph.D. Candidate in Computer Science *3/2016–present*
Università della Svizzera italiana, Lugano, Switzerland
- Thesis: Theory-aware Abstraction for Incremental Software Verification (working title)
- Advisor: Prof. Natasha Sharygina

M.Sc in Information Technology/ Secure Communications *9/2010–1/2013*
Iran University of Science & Technology (IUST), Tehran, Iran
- Thesis: Formal Verification of the Network Management Protocol SNMPv3 using ProVerif, GPA: 17.27/20

B.Sc Electrical Engineering/ Electronics *9/2004–10/2008*
Zanjan University, Zanjan, Iran
- Thesis: Design and Implementation of a logic circuit using Low-Power Techniques

Mathematics and Physics Diploma *9/2000–9/2004*
National Organization for Development of Exceptional Talents (NODET), Mianeh, Iran. Total GPA: 19/20

SKILLS

Programming Languages:	***Advanced:*** C++ | Python | Bash ***Familiar:*** HTML | Verilog | MATLAB
Software Development:	Programming Paradigms | testing | software versioning (SVN, Git)
Modeling Languages & Tools:	SMT-LIB | Promela | SPIN | ProVerif
Operating Systems:	Linux (Ubuntu, CentOS) | MacOS | Windows

INDUSTRY EXPERIENCE

R&D Engineer in MAT IT-Solutions, Tehran, Iran *2/2014–5/2015*
- Applied Public Key Infrastructure solutions for digitalizing the existing travel documents

Researcher in Iran Telecommunication Research Center (ITRC), Tehran, Iran *1/2013–12/2013*
- Our team offered road maps towards designing and implementing National Information Network

Intern in ICT Research Institute, Tehran, Iran *7/2012–12/2012*
- Contributed to formal evaluation and security assurance of network management protocols

FURTHER EDUCATION

Dependable Software Systems Engineering, Marktoberdorf School, Germany *8/2016*
SAT/SMT & Automated Reasoning Summer School, Lisbon, Portugal *6/2016*
SAT/SMT & Symbolic Computation Summer School, MPI Informatics, Saarbrücken, Germany *8/2017*
Computer Aided Verification, USI Lugano, Switzerland *2/2016–6/2016*

PUBLICATIONS

Incremental Verification by SMT-based Summary Repair *Accepted to FMCAD'20*
S. Asadi, M. Blicha, A. Hyvärinen, G. Fedyukovich, N. Sharygina

Farkas-Based Tree-Interpolation *Accepted to SAS'20*
S. Asadi, M. Blicha, A. Hyvärinen, G. Fedyukovich, N. Sharygina

Function Summarization Modulo Theories. *LPAR'18*
S. Asadi, M. Blicha, G. Fedyukovich,A. Hyvärinen, K. Even, N. Sharygina, H. Chockler

Lattice-Based Refinement in Bounded Model Checking. *VSTTE'18*
K. Even, S. Asadi, A. Hyvärinen, H. Chockler, N. Sharygina

Computing Exact Worst-Case Gas Consumption for Smart Contracts. *ISoLA'18*
M. Marescotti, M. Blicha, A. Hyvärinen, S. Asadi, N. Sharygina

Theory Refinement for Program Verification. *SAT'17*
A. Hyvärinen S. Asadi, K. Even, G. Fedyukovich, H. Chockler, N. Sharygina

HiFrog: SMT-based Function Summarization for Software Verification. *TACAS'17*
L. Alt, S. Asadi, H. Chockler, K. Even, G. Fedyukovich, A. Hyvärinen, N. Sharygina

Duality-based Interpolation for QF_EUF. *FMCAD'17*
L. Alt, A. Hyvärinen, S. Asadi, N. Sharygina

Formal Security Analysis of Authentication in SNMPv3 Protocol by an Automated Tool. *IST'12*
S. Asadi, H. Shahhoseini

HiFrog: Interpolation-based Software Verification using Theory Refinement. *Poster - FMCAD'17*
S. Asadi

TEACHING & INVITED TALKS

Teaching Assistant at USI Lugano *9/2016–present*
- Software Design and Modelling, Theory of Computation, Fundamentals of Informatics

Invited talk at 11th Alpine Verification Meeting (AVM), Hungary *9/2017*
- HiFrog: SMT-based Function Summarization for Software Verification

Invited talk at ITRC workshop *1/2012*
- A survey on formal verification approaches of security protocols

GRANTS, AWARDS, & HONOURRS

- Awarded ITRC Research Grant for my M.Sc. Thesis, 2013
- Student Travel Grants for attending conferences/summer schools awarded by NATO Science , SAT'17, FMCAD'17
- Selected as the top student in Young Mathematicians Contest in Mianeh, 1996
- Ranked among the top 1% of the participants of both undergraduate and graduate university entrance exams

COLLABORATIONS & ACADEMIC SERVICE

Florida State University, USA:	Collaboration with Prof. Grigory Fedyukovich	*2016–ongoing*
King's College London:	Collaboration with Prof. Hana Chockler	*2016–2018*
Journal Reviewer:	ACM Journal of Computing Surveys (CSUR)	
Conference Subreviewer:	CAV ('20, '19, '18); TACAS ('20, '18, '17); FM ('19, '18, '16); FMCAD ('19, '18, '17); VMCAI ('20); SAT ('20,'19); AAAI ('19); HVC ('17); MARS(20)	

SOFT SKILLS

Languages:	***native:*** Azeri | Persian ***fluent:*** English ***beginner:*** Italian
Communication:	public speaking | academic writing | ability to communicate own ideas
Teamwork:	cooperative | adaptable | experience with multicultural teams
Others:	enthusiastic | self-motivated | dedicated | detail-oriented
Hobbies:	listening to self-development podcasts | playing piano | movies | sweet making