

THE HIGHER ORDER HAUSDORFF VORONOI DIAGRAM AND VLSI CRITICAL AREA EXTRACTION FOR VIA-BLOCKS

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ABSTRACT. We extend the Voronoi diagram framework to compute the *critical area* of a circuit layout [15, 12, 16, 13, 14] with the ability to accurately compute critical area for *via-blocks* on via and contact layers in the presence of multilayer loops, redundant vias, and redundant interconnects. Critical area is a measure reflecting the sensitivity of a VLSI design to random defects during IC manufacturing. The method is based on concepts of the higher order Hausdorff Voronoi diagram of point clusters in the plane. We investigate structural properties of the order- k Hausdorff Voronoi diagram and present a simple iterative approach that computes the ordinary Hausdorff Voronoi diagram of iteratively determined clusters of points. We highlight simplifications in the L_∞ metric, a metric of practical interest in VLSI critical area extraction.

INTRODUCTION

The *Hausdorff Voronoi diagram* of a set S of point clusters in the plane is a subdivision of the plane into regions such that the *Hausdorff Voronoi region* of a cluster $P \in S$ is the locus of points *closer* to P than to any other cluster in S , where distance between a point t and a cluster P is measured according to the *Hausdorff distance*¹. The Hausdorff Voronoi region of P can be defined equivalently as the locus of points t whose maximum distance from any point in P is less than the maximum distance of t from any other cluster in S . The Hausdorff Voronoi region of P is subdivided into finer regions by the farthest-point Voronoi diagram of P . The Hausdorff Voronoi diagram has been studied in [6, 1, 13, 17, 5]. It has also been known as the *cluster Voronoi diagram* [6], and the *closest covered set diagram* [1].

In this paper we investigate the order k , $k \geq 1$, Hausdorff Voronoi diagram of point clusters in the plane as motivated by the problem of extracting *critical area* for *via-blocks* in a VLSI design. The maximum order Hausdorff Voronoi diagram of S simplifies to the farthest

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¹The (directed) Hausdorff distance from a set A to a set B is $h(A, B) = \max_{a \in A} \min_{b \in B} \{d(a, b)\}$. The (undirected) Hausdorff distance between A and B is $d_h(A, B) = \max\{h(A, B), h(B, A)\}$.

point Voronoi diagram of all points in S . Clusters of points can be arbitrary and they are allowed to form *crossing*² configurations. We present a simple iterative approach to compute the order k Hausdorff Voronoi diagram that computes the ordinary Hausdorff Voronoi diagram of iteratively determined clusters of points. To compute the ordinary Hausdorff Voronoi diagram we use the plane sweep algorithm of [13].

The k th order Hausdorff Voronoi diagram is used to model the VLSI *critical area* extraction problem for *via-blocks* in the presence of loops and redundant interconnects. *Critical area* is a measure reflecting the sensitivity of the design to random defects occurring during the manufacturing process (see e.g. [19, 18]). Reliable critical area extraction is essential for today's IC manufacturing especially when DFM, i.e., design for manufacturability, initiatives are under consideration.

Critical area on one layer of a circuit layout is defined as

$$A_c = \int_0^\infty A(r)D(r)dr$$

where $A(r)$ denotes the area in which the center of a defect of radius r must fall in order to cause a circuit failure and $D(r)$ is the density function of the defect size. $D(r)$ has been estimated as $D(r) = r_0^2/r^3$, where r_0 is some minimum optically resolvable size. There are two types of manufacturing faults causing circuit failure: *extra-material* defects, causing shorts between different conducting regions, and *missing material* defects causing open circuits. Missing material defects on conducting layers result in broken conducting paths, typically referred to as *opens*. Missing material defects on contact and via layers result in missing contacts (vias) between neighboring conducting layers and they are called *via-blocks*. This paper deals with critical area extraction for via-blocks extending the results of [12] with the ability to accurately compute critical area for via-blocks even in the presence of multilayer loops, redundant vias, and redundant interconnects.

In [12] the Hausdorff Voronoi diagram had been used to address the critical area extraction problem for via-blocks in a simplified setting where no redundant interconnects were assumed and as a result clusters of vias could be assumed to form *non-crossing* configurations and participate in no loops. In this paper we generalize the results of [12] and use the higher order Hausdorff Voronoi diagram and a modeling of a net as a compact graph given in [14] to accurately model and compute critical area for via-blocks on via and contact layers even in the presence of loops and redundant interconnects. Redundant interconnects creating loops that may span over a number of layers are increasingly

²Two clusters of points are called *crossing* if their convex hulls admit more than two common lines of support; otherwise they are called *non-crossing*. The convex hulls of non-crossing clusters of points are allowed to intersect.

inserted in a design in order to increase design reliability and reduce the potential for open circuits (see e.g. [8]). Redundant interconnects reduce the potential for open faults, at the expense however of increasing the potential for shorts. The ability to accurately evaluate critical area in all cases and perform trade-offs is important, especially when changes to enhance manufacturability and yield are performed in the design.

The Voronoi diagram approach to critical area extraction for various types of faults [15, 16, 12, 14] is based on the following idea: Subdivide the layout layer under consideration into regions such that critical area integration can be performed analytically within each region. Critical area integration becomes trivial once the appropriate Voronoi diagram is derived. The Voronoi approach on critical area extraction for various types of faults has been implemented into the IBM Voronoi Critical Area Analysis tool (*Voronoi CAA*) which is used extensively by IBM Microelectronics for the prediction of yield. For results on the early industrial use of our tool and comparisons with previously available tools see [11]. Previous approaches to extract critical area can be grouped into two major categories: Monte Carlo simulation (see e.g. [21, 18]) and *deterministic iterative methods* referred to as *shape shifting* techniques (see, e.g., [3, 7, 4, 22]). Statistical layout window sampling in combination with basic shape shifting techniques has been used in [2] to address critical area extraction at the chip level.

1. THE HIGHER ORDER HAUSDORFF VORONOI DIAGRAM OF POINT CLUSTERS IN THE PLANE

The *farthest distance* between a point t and a cluster of points P is $d_f(t, P) = \max\{d(t, p), p \in P\}$, where $d(t, p)$ denotes the ordinary distance between two points t, p . The Hausdorff distance between two clusters of points P and Q is $d_h(P, Q) = \max\{h(P, Q), h(Q, P)\}$, where $h(P, Q) = \{\max_{p \in P} \min_{q \in Q} d(p, q)\}$ denotes the (directed) Hausdorff distance from P to Q . The Hausdorff bisector between P and Q is $b_h(P, Q) = \{y \mid d_h(y, P) = d_h(y, Q)\}$ which is equivalent to the bisector between P and Q under the farthest distance function i.e., $b_h(P, Q) = \{y \mid d_f(y, P) = d_f(y, Q)\}$ [17]. The Hausdorff bisector is a subgraph of the farthest-point Voronoi diagram of the set $P \cup Q$ [17]. Figure 1 illustrates examples of $b_f(P, Q)$ in the L_∞ metric. In the L_∞ metric $d_f(t, P) = d_f(t, R)$ where R is the minimum enclosing rectangle of P . That is, in the L_∞ metric any cluster of points simplifies to a single rectangle corresponding to the minimum enclosing rectangle of the original point cluster. In Figure 1, solid lines indicate $b_h(P, Q)$ and dashed lines illustrate the farthest point Voronoi diagram of $P \cup Q$. The shaded region illustrates a region equidistant from both P and Q that can be assigned arbitrarily to one of the two.

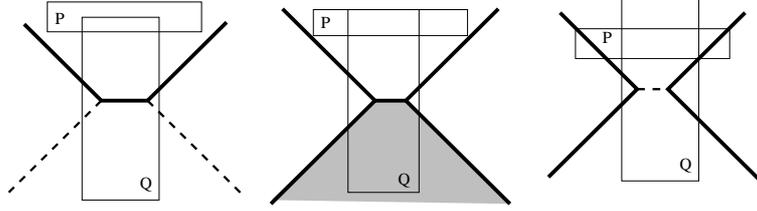


FIGURE 1. The Hausdorff bisector in the L_∞ metric.

Let S be a set of point clusters. The Hausdorff Voronoi region of cluster $P \in S$ is defined as

$$hreg(P) = \{x \mid d_f(x, P) < d_f(x, Q), \forall Q \in S\}$$

$hreg(P)$ may be disconnected and it is further partitioned into finer regions by the farthest point Voronoi diagram of P , denoted $f-Vor(P)$. For any point $p \in P$, $hreg(p) = \{x \mid d(x, p) = d_f(x, P) < d_f(x, Q), \forall Q \in S\}$. The collection of all (non-empty) Hausdorff Voronoi regions defined by S , together with their bounding edges and vertices, is called the *Hausdorff Voronoi diagram* of S . The structural complexity of the Hausdorff Voronoi diagram is $\Theta(n + m)$, where n is the total number of points on the convex hulls of all clusters, and m reflects the number of *crossings*³ among clusters in S . In the worst case, m is $O(n^2)$.

The k th order Hausdorff Voronoi diagram of S , denoted $h-Vor_k(S)$, is a subdivision of the plane into maximal regions such that each point t within a given region has the same k clusters as nearest neighbors. The distance between a point t and a cluster P is $d_f(t, P)$. The k th order Hausdorff Voronoi region of a k -tuple of clusters H is denoted as $h-reg(H)$. Let H' denote the collection of all points constituting the clusters in H that is, $H' = \{q \mid q \in Q, Q \in H\}$. Clearly, $d_f(t, H') = \max\{d_f(t, Q), Q \in H\}$. The collection of all clusters H' as induced by every region $h-reg(H)$ of $h-Vor_k(S)$ is denoted as S'_k . The following lemma is not hard to see.

Lemma 1. *The k th order Hausdorff Voronoi diagram of S , $h-Vor_k(S)$, is equivalent to the Hausdorff Voronoi diagram of S'_k , where S'_k denotes the collection of point clusters H' induced by every k th order Voronoi region $h-reg(H)$ of $h-Vor_k(S)$.*

Let's now define a *k th order set of point clusters*.

Definition 2. Given an initial set S of point clusters in the plane, the *k th order set of point clusters* S_k , $k \geq 1$, is defined as follows:

- (1) $S_1 = S$.
- (2) For any pair of clusters $H, R \in S_k$ with neighboring Voronoi regions in $h-Vor(S_k)$, let cluster $Q = H \cup R$ be in S_{k+1} . Cluster

³ m corresponds to the total number of *crucial supporting segments* between pairs of crossing clusters. See Def. 4 of [13].

R is called a *neighbor* of H . Also for any cluster $T \in S_k$ that is *crossing* either R or H , let $H \cup T$ be a cluster in S_{k+1} . T is called a *potential neighbor* of H . In other words, any point cluster $Q \in S_{k+1}$, is derived as the union of two point clusters H, R in S_k such that H, R are neighbors or potential neighbors in $h\text{-Vor}(S_k)$.

Lemma 3. *The k th order Hausdorff Voronoi diagram of a set of point clusters S is equivalent to the ordinary Hausdorff Voronoi diagram of the order k set of clusters S_k as defined in Def. 2. That is, $h\text{-Vor}_k(S) = h\text{-Vor}(S_k)$.*

The Hausdorff Voronoi diagram has three types of Voronoi vertices: ordinary Voronoi vertices where at least 3 Hausdorff bisectors meet, farthest Voronoi vertices as part of the inner finer subdivision of individual Hausdorff regions, and *mixed* Voronoi vertices corresponding to *breakpoints* of Hausdorff bisectors. A mixed Voronoi vertex encodes the special properties of the Hausdorff Voronoi diagram and corresponds to the meeting point of a single Hausdorff bisector $b_h(P, Q)$ and a farthest bisector of either $f\text{-Vor}(P)$ or $f\text{-Vor}(Q)$, see [13] for more details. It is interesting to note that the number of mixed Voronoi vertices does not increase with k , the order of the Hausdorff Voronoi diagram, unlike the ordinary Voronoi vertices (see Lemma 4). Note that vertices induced by more than one Hausdorff bisector are not considered mixed even if they are also incident to a farthest bisector.

Lemma 4. *The number of mixed Hausdorff Voronoi vertices in $h\text{-Vor}_k(S)$, $k \geq 1$, remains $O(n + m)$.*

Proof. The proof is based on the properties of mixed vertices along $T(P)$, the tree structure of the farthest Voronoi diagram of cluster P , as listed in Lemmas 2 and 4 of [13]. \square

By Lemma 4, the structural complexity analysis of [13, 17], and standard higher order Voronoi diagrams [9], it can be shown that the structural complexity of $h\text{-Vor}_k(S)$ is $O(kn + m)$. The maximum order Hausdorff Voronoi diagram of a set S of point clusters simplifies to the ordinary farthest point Voronoi diagram of all points in S .

Lemma 3 implies a simple iterative approach to compute higher order Hausdorff Voronoi diagrams: Given $h\text{-Vor}(S_k)$, $k \geq 1$, first derive S_{k+1} as defined in Def. 2; then compute $h\text{-Vor}(S_{k+1})$ which is exactly $h\text{-Vor}_{(k+1)}(S)$ by Lemma 3. To compute the ordinary Hausdorff Voronoi diagram of a set of point clusters, the plane sweep algorithm of [13] can be employed enhanced with the ability to deal with clusters of points that share common points.

Figure 2a, borrowed from [13], illustrates a Hausdorff Voronoi diagram of $S = \{P_1, P_2, P_3\}$. Figure 2b, illustrates the 2nd order Hausdorff Voronoi diagram of S . Dashed lines illustrate the subdivision of

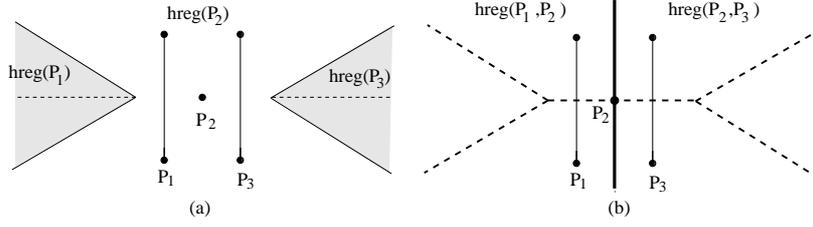


FIGURE 2. The 1st and 2nd order Hausdorff Voronoi diagram of $S = \{P_1, P_2, P_3\}$.

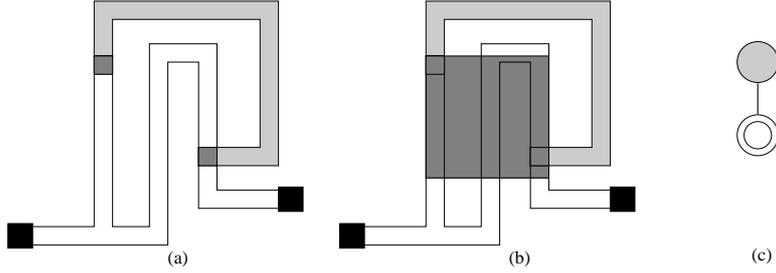


FIGURE 3. (a) A net N spanning over two layers. (b) A via-block for net N . (c) The corresponding compact graph.

$h-reg(P_1, P_2)$ and $h-reg(P_2, P_3)$ by the farthest point Voronoi diagram of $P_1 \cup P_2$ and $P_2 \cup P_3$ respectively.

2. MODELING VIA-BLOCKS IN A VLSI LAYOUT

A net in a VLSI layout corresponds to a collection of interconnected shapes spanning over a number of layers. Some of the shapes are designated as *terminal shapes* representing the entities that the net must interconnect. A net remains *functional* as long as all its terminal shapes remain interconnected. Otherwise the net gets *broken*. On each conducting layer a net consists of a number of connected components referred to as *wires*. Two connected components on neighboring conducting layers get connected through *vias* (resp. contacts) on the in-between via (resp. contact) layer. A via or contact corresponds to a small square shape. A collection of vias connecting the same pair of wires on neighboring conducting layers are called *redundant* and they form a *via-cluster*. Figure 3(a), borrowed from [14], illustrates a simple net spanning over two metal layers, M1 and M2, where M2 is illustrated shaded. The two contacts illustrated as black squares have been designated as terminal shapes. The two vias, shown as gray squares connecting wires on layers M1 and M2 form a group of redundant vias i.e., a via-cluster.

Given a net N , a compact graph representation $G(N)$ was presented in [14] as follows: Every connected component of N on a conducting

layer is represented by a graph node in $G(N)$. A node containing terminal shapes is designated as a terminal node. Two graph nodes are connected by an edge if there exists at least one via connecting the respective components of N (unless they form a transistor). Any number of vias connecting the same pair of connected components forms a group of *redundant* vias. To build $G(N)$ some net extraction capability needs to be available. Net extraction is a well studied topic beyond the scope of this paper. Similarly to [14] we assume that $G(N)$ can be available for any net. The compact graph representation of the example in Figure 3(a) is shown in Figure. 3(c); the double circle indicates a terminal node.

Let $G(N, V)$ denote the subset of edges in $G(N)$ corresponding to vias on a via or contact layer V . Each edge of $G(N, V)$ corresponds to a group of redundant vias (maybe only a single via) that constitute a via-cluster. A defect destroying the entire via-cluster corresponds to deleting the corresponding edge of $G(N, V)$. If deleting this edge disconnects $G(N)$ leaving terminal nodes in two sides the defect forms a *via-block*.

Definition 5. A *via-block* on a via or contact layer V is a disk D that entirely overlaps one or more via clusters i.e., an entire group (resp. groups) of redundant vias, on layer V such that the corresponding set of graph edges in $G(N, V)$ forms a *cut*. A cut is a collection of edges in $G(N, V)$ whose removal disconnects $G(N)$ leaving terminal nodes in at least two sides.

The above definition is based on the via-block model given in [10, 21] enhanced with the consideration of multilayer loops. Figure 3(b) illustrates a via block in the L_∞ metric; it is shown as a gray square overlapping a cluster of two vias.

$G(N)$ can be partitioned into *biconnected components*, *bridges* and *articulation points* in linear time [20]. A bridge is an edge whose removal disconnects $G(N)$. A bridge is *trivial* if its removal does not disconnect any terminal nodes of $G(N)$. A defect destroying entirely the via-cluster corresponding to a non-trivial bridge forms a via-block. A defect destroying the via-cluster corresponding to an edge of a biconnected component results in no fault unless it destroys a number of via-clusters corresponding to a number of edges in $G(N, V)$ forming a cut.

3. THE HIGHER ORDER HAUSDORFF VORONOI DIAGRAM FOR VIA-BLOCKS

Let V be a via layer and S be a set of via-clusters on V . The Voronoi approach to compute critical area for via-blocks on V asks for a subdivision of V into regions that reveal the *critical radius* for every point t on V . The critical radius at a point t , $r_c(t)$ is the radius of

the smallest defect centered at t causing a via-block. We refer to this subdivision as the *Voronoi diagram for via-blocks on layer V* .

Without loss of generality we can assume that $G(N, V)$ contains no trivial bridges as any via cluster corresponding to a trivial bridge of $G(N, V)$ can simply be discarded from S . If $G(N, V)$ participates in no biconnected component then any via-cluster on V corresponds to a bridge of $G(N)$ forming a *cut*. In the presence of biconnected components we say that a tuple of via-clusters H forms a *cut* if the set of corresponding edges in $G(N, V)$ forms a cut of $G(N)$. If in addition no proper subset of H forms a cut, H is said to form a *minimal cut*. Any tuple of via clusters corresponding to a minimal cut is colored red and for brevity we refer to it as a *red tuple of clusters*.

Lemma 6. *Let $h\text{-Vor}_k(S)$ be a k th order Hausdorff Voronoi diagram of S , $k \geq 1$. Let $h\text{-reg}(H)$ be the region of a k -tuple H of via clusters such that H corresponds to a minimal cut (if any). Then the critical radius for via-blocks for any point $t \in h\text{-reg}(H)$ is $r_c(t) = d_f(t, H)$.*

If $G(N, V)$ contains no portion of a biconnected component of $G(N)$ then Lemma 6 implies that the Voronoi diagram for via-blocks is equivalent to the Hausdorff Voronoi diagram of S , $h\text{-Vor}(S)$. Otherwise Lemma 6 implies an iterative process to compute the Voronoi diagram for via-blocks based on properties of the higher order Hausdorff Voronoi diagram. Let S_k be an iteratively determined set of via clusters as follows: $S_1 = S$. All red via-clusters in S_k (i.e. via-clusters corresponding to minimal cuts) are included in S_{k+1} . For any pair of non-red via clusters H, R in S_k that are neighbors or potential neighbors in $h\text{-Vor}(S_k)$ (if any), let $Q = H \cup R$ be a new via cluster in S_{k+1} . No other cluster is included in S_{k+1} .

Theorem 7. *The Hausdorff Voronoi diagram of S_r , $h\text{-Vor}(S_r)$, where r is the minimum index for which all clusters in collection $S_k, k \geq 1$ are colored red, corresponds to the Voronoi diagram for via-blocks on layer V . That is, for any point t in $h\text{-reg}(H)$ in $h\text{-Vor}(S_r)$, $r_c(t) = d_f(t, H)$, $H \in S_r$.*

A remaining question is to determine whether a new via-cluster $Q \in S_{k+1} - S_k$ corresponds to a cut of $G(N)$. For cuts of size 1 and 2 the question can be answered efficiently by determining biconnected and triconnected components of $G(N)$ respectively. For larger cuts a straightforward approach given in [14] can be used, adding however a quadratic factor in the total asymptotic time complexity. In practice the size of relevant cuts is expected to remain very small.

The construction of the Hausdorff Voronoi diagram and therefore the construction of the Voronoi diagram for via-blocks can be done by plane sweep as described in [13]. In the L_∞ metric the main concepts remain the same but the algorithm simplifies considerably. Recall that

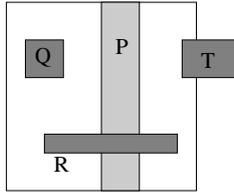


FIGURE 4. Example of clusters interacting with P .

via clusters in L_∞ correspond to rectangles. The union of two via clusters corresponds to deriving the minimum enclosing rectangle of a pair of rectangles. The details are given in the full paper.

Definition 8. In L_∞ two via clusters are called interacting if the minimum enclosing rectangle of one is entirely contained into a minimum enclosing square of the other.

Figure 4 illustrates examples of pairs of interacting clusters in the L_∞ metric. Clusters Q, R, T are all interacting with P . Note that, although not shown in Figure 4, T is also enclosed in some minimum enclosing square of P .

Theorem 9. *The L_∞ Hausdorff Voronoi diagram of a set of via clusters can be computed by plane sweep in time $O((N + K) \log N)$, where N denotes the number of via clusters, and K denotes the number of pairs of interacting clusters.*

In the L_∞ metric, once the Voronoi diagram for via-blocks is derived critical area integration can be done analytically as shown in [12].

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REFERENCES

1. M. Abellanas, G. Hernandez, R. Klein, V. Neumann-Lara, and J. Urrutia, *A combinatorial property of convex sets*, Discrete Computat. Geometry **17** (1997), 307–318.
2. G. A. Allan, *Yield prediction by sampling IC layout*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **19** (2000), no. 3, 359–371.
3. G. A. Allan and A.J. Walton, *Efficient extra material critical area algorithms*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **18** (1999), no. 10, 1480–1486.
4. J. Pineda de Gyvez and C. Di, *IC defect sensitivity for footprint-type spot defects*, IEEE Trans. on Computer-Aided Design **11** (1992), no. 5, 638–658.

5. Frank Dehne, Anil Maheshwari, and Ryan Taylor, *A coarse grained parallel algorithm for Hausdorff Voronoi diagrams*, Proc. 2006 International Conference on Parallel Processing, 2006, pp. 497–504.
6. H. Edelsbrunner, L.J. Guibas, and M. Sharir, *The upper envelope of piecewise linear functions: Algorithms and applications*, Discrete Computat. Geometry **4** (1989), 311–336.
7. A. L. Jee and F.J. Ferguson, *CARAFE: An inductive fault analysis tool for CMOS VLSI circuit*, Proc. IEEE VLSI Test Symposium, 1992, pp. 92–98.
8. A. B. Kahng, B. Liu, and I. I. Mandoiu, *Non-tree routing for reliability and yield improvement*, IEEE Trans. on Comp. Aided Design of Integrated Circuits and Systems **23** (2004), no. 1, 148 – 156.
9. D. T. Lee, *On k -nearest neighbor Voronoi diagrams in the plane*, IEEE Trans. Comput. **C-31** (1982), no. 6, 478–487.
10. B. R. Mandava, *Critical area for yield models*, Tech. report, IBM Technical Report TR22.2436, January 1982.
11. D. N. Maynard and J. D. Hibbeler, *Measurement and reduction of critical area using Voronoi diagrams*, Advanced Semiconductor Manufacturing IEEE Conference and Workshop, 2005.
12. E. Papadopoulou, *Critical area computation for missing material defects in VLSI circuits*, IEEE Transactions on Computer-Aided Design **20** (2001), no. 5, 583–597.
13. ———, *The Hausdorff Voronoi diagram of point clusters in the plane*, Algorithmica **40** (2004), 63–82.
14. ———, *Higher order Voronoi diagrams of segments for VLSI critical area extraction*, Proc. 18th International Symposium on Algorithms and Computation, Lecture Notes in Computer Science 4835, vol. 4835, 2007, pp. 716–727.
15. E. Papadopoulou and D. T. Lee, *Critical area computation via Voronoi diagrams*, IEEE Transactions on Computer-Aided Design **18** (1999), no. 4, 463–474.
16. E. Papadopoulou and D.T. Lee, *The l_∞ Voronoi diagram of segments and VLSI applications*, International Journal of Computational Geometry and Applications **11** (2001), no. 5, 503–528.
17. ———, *The Hausdorff Voronoi diagram of polygonal objects: A divide and conquer approach*, International Journal of Computational Geometry and Applications **14** (2004), no. 6, 421–452.
18. C. H. Stapper, *Modeling of defects in integrated circuit photolithographic patterns*, IBM J. Res. Develop. **28** (1984), no. 4, 461–475.
19. C. H. Stapper and R. J. Rosner, *Integrated circuit yield management and yield analysis: Development and implementation*, IEEE Trans. Semiconductor Manufacturing **8** (1995), no. 2, 95–102.
20. R. Tarjan, *Depth-first search and linear graph algorithms*, SIAM Journal on Computing **1** (1972), 146–160.
21. H. Walker and S. W. Director, *VLASIC: A yield simulator for integrated circuits*, IEEE Trans. on Computer-Aided Design **5** (1986), no. 4, 541–556.
22. S. T. Zachariah and S. Chakravarty, *Algorithm to extract two-node bridges*, IEEE Transactions on VLSI Systems **11** (2003), no. 4, 741–744.

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