Higher order Voronoi diagrams of segments for VLSI critical area extraction*

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We address the problem of computing critical area for open faults in a circuit layout in the presence of multilayer loops and redundant interconnects. The extraction of critical area is a fundamental problem in VLSI yield prediction. We first model the problem as a graph problem and then we solve it efficiently by exploiting its geometric nature. We introduce the *open-fault Voronoi diagram of polygonal objects*, a generalization of Voronoi diagrams based on concepts of higher order Voronoi diagrams of segments. Once this Voronoi diagram is available the entire critical area integral for open faults can be computed analytically in linear time similarly to [7, 8, 5]. This paper expands the Voronoi critical area computation paradigm [7, 5, 6] with the ability to accurately compute critical area for missing material defects even in the presence of loops and redundant interconnects spanning over multiple layers.

Catastrophic yield loss of integrated circuits is caused to a large extent by random particle defects interfering with the manufacturing process resulting in functional failures such as open or short circuits. All yield models for random manufacturing defects focus on critical area, a measure reflecting the sensitivity of the design to random defects during manufacturing (see e.g. [9]). The critical area of a circuit layout on a layer A is defined as

$$A_c = \int_0^\infty A(r)D(r)dr$$

where $A(r)$ denotes the area in which the center of a defect of radius r must fall in order to cause a circuit failure and $D(r)$ is the density function of the defect size. $D(r)$ has been estimated as $D(r) = r_0^2/r^3$, where r_0 is some minimum optically resolvable size. Critical area analysis is typically performed on a per layer basis and results are combined to estimate total yield.

In this paper we focus on critical area extraction for *open faults*, also called *opens*, resulting from broken interconnects generalizing upon the results of [5]. Opens are net-aware, that is, a defect is considered a fault only if it actually *breaks* a net. A net N is a collection of interconnected shapes spanning over a number of layers. Some of the shapes are designated as *terminal shapes* representing the entities that the net must interconnect. A net is said to be *broken* if there exist terminal shapes that get disconnected or destroyed. In order to increase design reliability and reduce the potential for open circuits designers are increasingly introducing redundant interconnects creating interconnect loops that may span over a number of layers (see e.g. [2]). Redundant interconnects reduce the potential for open faults at the expense of increasing the potential for shorts. The ability to perform trade-offs is important requiring accurate critical area computation for both.

We formalize the notion of an *open* as follows: A *minimal open* is a defect D that breaks a net N and D has minimal size, that is, if D is shrunk by $\epsilon > 0$ then D no longer breaks N. D breaks N if any two terminal shapes of N get disconnected or if a terminal shape itself gets destroyed. An *open* is any defect entirely covering a minimal open. Given a layer A where critical area analysis needs to be performed, we define the *opens Voronoi diagram* on layer A as a subdivision of the layer into regions such that each region reveals the *critical radius* for opens for every point in that region. The critical radius of a point t, $r_c(t)$, is the size of the smallest defect centered at t causing

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a circuit failure. A circuit failure corresponds to an open. For any point t in a region $reg(h)$ of the opens Voronoi diagram the critical radius of t corresponds to a distance function from the owner h, specifically $r_c(t) = d_w(t, h)$, where $d_w(t, h)$ denotes a (weighted) distance between t and h.

We model each net N as a graph extended with portions of the medial axis of shapes on layer A constituting N, denoted as $G(N, A)$. The elements of the medial axes contributing to $G(N, A)$ are referred to as *core elements*. A *cut* for net N is a collection of core elements whose removal *breaks* $G(N, A)$, i.e, it disconnects the graph leaving terminal points in at least two sides. We formulate the opens Voronoi diagram on layer A as a higher order Voronoi diagram of *core elements* on layer A that induce cuts. We propose an iterative process to compute the opens Voronoi diagram based on the iterative approach to compute higher order Voronoi diagrams of points [3]. We modify the iterative algorithm to accommodate (weighted) segments and the additional characteristics of the opens Voronoi diagram. To the best of our knowledge higher order Voronoi diagrams of segments had not received much attention in the literature with the recent exception of [1] for the farthest segment Voronoi diagram. The problem can have different flavors depending on whether segments are treated as closed entities or whether the open portions of segments are treated as distinct from their endpoints. In this paper we only deal with the latter interpretation as this is the one modeling our application. The Voronoi diagram for open faults can also be regarded as a Hausdorff Voronoi diagram of a set of cuts [6] (see e.g. [6] for the definition of the Hausdorff Voronoi diagram).

The algorithms presented in this paper have been integrated into the IBM Voronoi Critical Area Analysis tool (*Voronoi CAA*) which is used extensively by IBM manufacturing for the prediction of yield. For results on the industrial use of our tool and comparisons with previously available tools see [4].

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References

[1] F. Aurenhammer, R.L.S. Drysdale, and H. Krasser. Farthest line segment Voronoi diagrams. *Information Processing Letters*, (100):220–225, 2006.

[2] A. B. Kahng, B. Liu, and I. I. Mandoiu. Non-tree routing for reliability and yield improvement. *IEEE Trans. on Comp. Aided Design of Integrated Circuits and Systems*, 23(1):148 – 156, 2004.

[3] D. T. Lee. On k-nearest neighbor Voronoi diagrams in the plane. *IEEE Trans. Comput.*, C-31(6):478–487, June 1982.

[4] D. N. Maynard and J. D. Hibbeler. Measurement and reduction of critical area using Voronoi diagrams. In *Advanced Semiconductor Manufacturing IEEE Conference and Workshop*, 2005.

[5] E. Papadopoulou. Critical area computation for missing material defects in VLSI circuits. *IEEE Transactions on Computer-Aided Design*, 20(5):583–597, 2001.

[6] E. Papadopoulou. The Hausdorff Voronoi diagram of point clusters in the plane. *Algorithmica*, 40:63–82, 2004.

[7] E. Papadopoulou and D. T. Lee. Critical area computation via Voronoi diagrams. *IEEE Transactions on Computer-Aided Design*, 18(4):463–474, 1999.

[8] E. Papadopoulou and D.T. Lee. The l_∞ Voronoi diagram of segments and VLSI applications. *International Journal of Computational Geometry and Applications*, 11(5):503–528, 2001.

[9] C. H. Stapper and R. J. Rosner. Integrated circuit yield management and yield analysis: Development and implementation. *IEEE Trans. Semiconductor Manufacturing*, 8(2):95–102, May 1995.