Evanthia Papadopoulou

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RESEARCH INTERESTS

Design and Analysis of Algorithms, Computational Geometry and its Applications, Robust Geometric Computing, Data Structures, Algorithmic Aspects of VLSI Computer-Aided Design & Design for Manufacturability.

EDUCATION

Northwestern University, Department of EE/CS — Evanston, IL, USA
Ph.D. in Computer Science, December 1995.
Thesis title: Path Optimization in Combined Metrics.
Advisor: Professor D.T. Lee. GPA: 4.0/4.0.

University of Illinois at Chicago — Chicago, IL
Master of Science in Computer Science, December, 1989. GPA: 4.92/5.0.

University of Athens, Department of Mathematics — Athens, Greece
Bachelor of Science in Mathematics, June, 1986.

PROFESSIONAL EXPERIENCE

Università della Svizzera italiana (USI) — Lugano, Switzerland
Professor — 9/2016 – present
Associate Professor — 9/2008 – 8/2016

IBM T.J. Watson Research Center — Yorktown Heights, NY, USA
Research Staff Member — 1998 – 2008 (on leave academic years 2006–2008)
Postdoctoral Research Fellow — 9/1996 – 4/1998

Athens University of Economics and Business — Athens, Greece
Assistant Professor — 2004, 2006 – 2008 (tenure in 2007)

Northwestern University Evanston, IL, USA
Postdoctoral Researcher 1/1996 – 7/1996
Instructor, **Teaching Assistant**, **Research Assistant** 1990 – 1995

University of Illinois at Chicago Chicago, IL, USA
Visiting Lecturer, Teaching Assistant 1988 – 1990

FUNDING

SNF/DACH project 200021E-154387 – VORONOI++, 2016-2019. Funding 198'008 CHF.

Hasler Foundation project 16006 – EuroCG 2016, 2016. Funding CHF 7,050.
SNF 20CO21-164483, for the support of invited speakers, EuroCG 2016.

ESF/SNF project 20GG21-134355 – Hausdorff and Higher-order Voronoi diagrams, 2011-2015. Funding: 295'050 CHF. Part of the collaborative European Science Foundation (ESF) research project EuroGIGA/VORONOI.

SNF project 200020-149658 – Higher order Voronoi diagrams of polygonal objects, 2013-2014. Funding 57'160 CHF.

SNF project 200021-127137 – Generalized Voronoi diagrams of polygonal objects: algorithms and applications, 2010-2013. Funding: 157'692 CHF.

AWARDS

- IBM Technical Accomplishment for "Voronoi diagram based Critical Area Analysis", December 2006.
- IBM Outstanding Innovation Award for "Voronoi diagram based Critical Area Analysis", August 2006.
- IBM Invention Achievement Awards: Third Plateau September 2007, Second Plateau March 2005, First Plateau July 1999, First Patent Application May 1998.
- IBM Research Division Award, for the "Development and deployment of MASH", December 1999.

SHORT-TERM RESEARCH VISITS

- Courant Institute, New York University, NY, USA (6-7/2014, 7/2015, 11/2016, 6-7/2017)
- Universitat Politècnica de Catalunya (UPC), Spain (1/2013, 4/2017)
- Technion, Israel (10/2014)
- University of Bonn, Germany (7/2011, 7/2012)
- Bellairs Research Institute of McGill University, Barbados (2/2001, 1/2011, 3/2015)
- Academia Sinica, Taiwan, R.O.C (6-8/1993, 6/1996)

ADVISING POST-DOCTORAL FELLOWS

- Dr. Panagiotis Cheilaris, as a postdoctoral researcher through the EuroCIGA/VORONOI project SNF 20GG21-134355, 2011-2014.

ADVISING PHD STUDENTS

- Maksym Zavershyskyi. Higher-Order Voronoi Diagrams of Polygonal Objects, PhD dissertation, Faculty of Informatics, Università della Svizzera italiana, Lugano, Switzerland, December 2014.
  After graduation at: Google - Zurich.
- Sandeep Kumar Dey. Voronoi Diagrams in the Max-norm: Algorithms, Implementation, and Applications, PhD dissertation, Faculty of Informatics, Università della Svizzera italiana, Lugano, Switzerland, June 2015.
  After graduation at: Intel, Portland OR, USA
- Elena Khramtcova. Hausdorff, Farthest, and Cluster Voronoi diagrams, PhD dissertation, Faculty of Informatics, Università della Svizzera italiana, Lugano, Switzerland, August 2016.
  After graduation postdoc at: Université Libre de Bruxelles
- Kolja Junginger. Started September 2015.
- Martin Suderland. Started September 2016.
- Ioannis Mantas. Started October 2016.

COMMUNITY SERVICE

Conference Organization

- Conference Chair, 32nd European Workshop on Computational Geometry (EuroCG), Lugano, Switzerland, March 29 - April 1, 2016.
- Kickoff meeting of the ESF project EuroGIGA/VORONOI at USI, Lugano, October 7-11, 2011.

Membership in Program Committees

- Program-Committee Member, 29th International Symposium on Algorithms and Computation (ISAAC), Jiaoxi, Taiwan, December, 2018.
- Program-Committee Member, 34th European Workshop on Computational Geometry (EuroCG), Berlin, Germany, March 2018.
- Program-Committee Member, 33rd International Symposium on Computational Geometry (SoCG), Brisbane, Australia, July 1-4, 2017.
- Program-Committee co-Chair, 32nd European Workshop on Computational Geometry (EuroCG), Lugano, Switzerland, March 29 - April 1, 2016.
- Program-Committee Member, 27th International Symposium on Algorithms and Computation (ISAAC) Sydney, Australia, December, 2016.

- Program-Committee Member, 31st European Workshop on Computational Geometry (EuroCG), Ljubljana, Slovenia, March 2015.
- Program-Committee Member, 30th European Workshop on Computational Geometry (EuroCG), Ein Gedi, Israel, March 2014.
- Program-Committee Member, 24th International Symposium on Algorithms and Computation (ISAAC), Hong Kong, December 2013.
- Program-Committee Member, 10th International Symposium on Voronoi Diagrams in Science and Engineering (ISVD), Saint Petersburg, Russia, July 2013.
- Program-Committee Member, 7th International Symposium on Voronoi Diagrams in Science and Engineering (ISVD), Quebec City, Canada, June 2010.

Referee Activity

- International Journals (multiple times):

  Algorithmica (ALGO), SIAM Journal on Computing (SICOMP), Computational Geometry: Theory and Applications (CGTA), Computer Aided Geometric Design (CAGD), Discrete Applied Mathematics (DAM), Discrete and Computational Geometry (DCG), IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Information Processing Letters (IPL), International Journal of Computational Geometry and Applications (IJCGA), International Journal of Computer Mathematics, Networks, Wireless Communications and Mobile Computing.

- International Conferences (peer reviewed; multiple years):

  International Symposium on Computational Geometry (SoCG), European Symposium on Algorithms (ESA), International Symposium on Algorithms and Computation (ISAAC), International Computing and Combinatorics Conference (COCOON), International Symposium on Voronoi diagrams in Science and Engineering (ISVD), Symposium on Theoretical Aspects of Computer Science (STACS), International Workshop on Algorithms and Computation (WALCOM), European Workshop on Computational Geometry (EuroCG), Eurographics, IEEE Design Automation Conference (DAC).

TEACHING

Università della Svizzera italiana (USI) Lugano, Switzerland

Bachelor courses (designed and taught):
- Discrete Mathematics I: one semester each academic year, 2008–2014.
- Discrete Mathematics II: Spring 2009.
- Algorithms and Data Structures II (Topics in Algorithms): Fall 2010; one semester per academic year, 2012–present.

Master courses (designed and taught):
- Algorithms and Complexity: one semester per academic year, 2015 – present.
- Geometric Algorithms (Introduction to Computational Geometry): one semester per academic year, 2012 – present.

PhD courses:
- Introduction to Computational Geometry: Spring 2009; joint with Master Geometric Algorithms one semester per academic year, 2012 – present.
- Topics in Algorithms and Data Structures: Fall 2010.

Athens University of Economics and Business Athens, Greece

Undergraduate courses:
- Computer Graphics: Spring 2004, Fall 2004.
- Data Structures: Fall 2006, 2007.
- Automata and Complexity: Spring 2007, 2008.

Graduate courses:
- Automata and Complexity: Spring 2004.
- Graphics and Computational Geometry: Fall 2004, 2006, 2007.

Northwestern University Evanston, IL, USA
- EECS A20 - Introduction to Computers and Information Technology, three quarters per academic year, 1993 – 1995.

University of Illinois at Chicago Chicago, IL, USA
- Math191 - Structured Programming with Pascal I, 1989 – 1990.

PUBLICATIONS

Book Chapters

[1] E. Papadopoulou, J. Xu, and L. Xu. Map of geometric minimal cuts with applications. In P. M. Pardalos, D. Z. Du, and R. Graham, editors, *Handbook of Combinatorial Optimization*. Springer, 2nd edition, 2013.

[2] P. Gupta and E. Papadopoulou. Yield analysis and optimization. In C.J. Alpert, D.P. Mehta, and S.S. Sapatnekar, editors, *The Handbook of Algorithms for VLSI Physical Design Automation*, chapter 7.3. Taylor & Francis CRC Press, 2008.

Refereed Papers in Journals

[3] M. Claverol, E. Khramtcova, E. Papadopoulou, M. Saumell, and C. Seara. Stabbing circles for sets of segments in the plane. *Algorithmica*, 80(3):849884, March 2018. Special Issue on Theoretical Informatics.

[4] C. Bohler, C. H. Liu, E. Papadopoulou, and M. Zavershynskyi. A randomized divide and conquer algorithm for higher-order abstract Voronoi diagrams. *Computational Geometry: Theory and Applications*, 59(C):26–38, December 2016.

[5] P. Cheilaris, E. Khramtcova, S. Langerman, and E. Papadopoulou. A randomized incremental approach for the Hausdorff Voronoi diagram of non-crossing clusters. *Algorithmica*, 76(4):935–960, December 2016.

[6] S. K. Dey, P. Cheilaris, M. Gabrani, and E. Papadopoulou. Layout pattern analysis using the Voronoi diagram of line segments. *Journal of Micro/Nanolithography, MEMS, and MOEMS*, 15(1), February 2016.

[7] C. Bohler, P. Cheilaris, R. Klein, C. H. Liu, E. Papadopoulou, and M. Zavershynskyi. On the complexity of higher order abstract Voronoi diagrams. *Computational Geometry: Theory and Applications*, 48(8):539–551, September 2015.

[8] E. Papadopoulou and M. Zavershynskyi. The higher-order Voronoi diagram of line segments. *Algorithmica*, 74(1):415–439, 2016.

[9] E. Papadopoulou and J. Xu. The L_∞ Hausdorff Voronoi diagram revisited. *International Journal of Computational Geometry and Applications*, 25(2):123–141, 2015.

[10] C.-H. Liu, E. Papadopoulou, and D. T. Lee. The k-Nearest-Neighbors Voronoi diagram revisited. *Algorithmica*, 71(2):429–449, February 2015.

[11] J. Xu, L. Xu, and E. Papadopoulou. Computing the map of geometric minimal cuts. *Algorithmica*, 68:805–834, 2014.

[12] E. Papadopoulou and S. K. Dey. On the farthest line-segment Voronoi diagram. *International Journal of Computational Geometry and Applications*, 23(6):443–459, 2013.

[13] E. Papadopoulou. Net-aware critical area extraction for opens in VLSI circuits via higher-order Voronoi diagrams. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 30(5):704–716, 2011.

[14] Z. Chen, E. Papadopoulou, and J. Xu. Robustness of k-gon Voronoi diagram construction. *Information Processing Letters*, 97(4):138–145, 2006.

[15] E. Papadopoulou. The Hausdorff Voronoi diagram of point clusters in the plane. *Algorithmica*, 40:63–82, 2004.

[16] E. Papadopoulou and D. T. Lee. The Hausdorff Voronoi diagram of polygonal objects: A divide and conquer approach. *International Journal of Computational Geometry and Applications*, 14(6):421–452, 2004.

[17] E. Papadopoulou and D. T. Lee. The L_∞ Voronoi diagram of segments and VLSI applications. *International Journal of Computational Geometry and Applications*, 11(5):503–528, 2001.

[18] E. Papadopoulou. Critical area computation for missing material defects in VLSI circuits. *IEEE Transactions on Computer-Aided Design*, 20(5):583–597, May 2001.

[19] E. Papadopoulou. k-Pairs non-crossing shortest paths in a simple polygon. *International Journal of Computational Geometry and Applications*, 9(6):533–552, December 1999.

[20] O. Aichholzer, F. Aurenhammer, D. Chen, D. T. Lee, and E. Papadopoulou. Skew Voronoi diagrams. *International Journal of Computational Geometry and Applications*, 9(3):235–248, June 1999.

[21] E. Papadopoulou and D. T. Lee. Critical area computation via Voronoi diagrams. *IEEE Transactions on Computer-Aided Design*, 18(4):463–474, April 1999.

[22] E. Papadopoulou and D. T. Lee. A new approach for the geodesic Voronoi diagram of points in a simple polygon and other restricted polygonal domains. *Algorithmica*, 20(4):319–352, April 1998.

[23] D. T. Lee and E. Papadopoulou. The all-pairs quickest path problem. *Information Processing Letters*, 45:261–267, April 1993.

Journal Submissions

[24] E. Khramtcova and E. Papadopoulou. Randomized incremental construction for the Hausdorff Voronoi diagram revisited and extended. Invited submission to Journal of Combinatorial Optimization, special issue on Computing and Combinatorics, October 2017.

Pre-prints

[25] E. Khramtcova and E. Papadopoulou. An expected linear-time algorithm for the farthest-segment Voronoi diagram. arXiv:1411.2816v3 [cs.CG], 2017.

Refereed Papers in Conference Proceedings

[26] K. Junginger and E. Papadopoulou. Deletion in abstract Voronoi diagrams in expected linear time. In *Proc. 34th International Symposium on Computational Geometry (SoCG)*, June 2018.

[27] E. Khramtcova and E. Papadopoulou. Randomized incremental construction for the Hausdorff Voronoi diagram revisited and extended. In *Proc. 23rd Annual International Computing and Combinatorics Conference (COCOON)*, volume 10392 of *LNCS*, pages 321–332, July 2017.

[28] H. Bennett, E. Papadopoulou, and C. Yap. Planar minimization diagrams via subdivision with applications to anisotropic Voronoi diagrams. In *Eurographics Symposium on Geometry Processing*, volume 35, June 2016.

[29] M. Claverol, E. Khramtcova, E. Papadopoulou, M. Saumell, and C. Seara. Stabbing circles for sets of segments in the plane. In *Proc. 12th Latin American Theoretical INformatics Symposium (LATIN)*, volume 9644 of *LNCS*, pages 290–305, April 2016.

[30] E. Khramtcova and E. Papadopoulou. Linear-time algorithms for the farthest segment Voronoi diagram and related tree-structures. In *Proc. 26th International Symposium on Algorithms and Computation (ISAAC)*, volume 9472 of *LNCS*, pages 404–414, December 2015.

[31] S. K. Dey, P. Cheilaris, N. Casati, M. Gabrani, and E. Papadopoulou. Topology and context-based pattern extraction using line-segment Voronoi diagrams. In *Proc. SPIE Advanced Lithography, Design-Process-Technology Co-optimization for Manufacturability IX*, volume 9427, March 2015. **Luigi Franco Cerrina Memorial Best Student Paper Award**.

[32] C. Bohler, C. H. Liu, E. Papadopoulou, and M. Zavershynskyi. A randomized divide and conquer algorithm for higher-order abstract Voronoi diagrams. In *Proc. 25th International Symposium on Algorithms and Computation (ISAAC)*, volume 8889 of *LNCS*, pages 27–37, December 2014.

[33] P. Cheilaris, S. K. Dey, M. Gabrani, and E. Papadopoulou. Implementing the L_∞ segment Voronoi diagram in CGAL and applying in VLSI pattern analysis. In *Proc. 4th International Congress on Mathematical software (ICMS)*, volume 8592 of *LNCS*, pages 198–205, 2014.

[34] P. Cheilaris, E. Khramtcova, S. Langerman, and E. Papadopoulou. A randomized incremental approach for the Hausdorff Voronoi diagram of non-crossing clusters. In *Proc. 11th Latin American Theoretical INformatics Symposium (LATIN)*, volume 8392 of *LNCS*, pages 96–107, March 2014.

[35] G. Barequet and E. Papadopoulou. On the farthest Voronoi diagram of line segments in three dimensions. In *Proc. 10th International Symposium on Voronoi Diagrams in Science and Engineering (ISVD)*, pages 31–36. IEEE-CS, July 2013.

[36] M. Zavershynskyi and E. Papadopoulou. A sweepline algorithm for higher order Voronoi diagrams. In *Proc. 10th International Symposium on Voronoi Diagrams in Science and Engineering, (ISVD)*, pages 16–22. IEEE-CS, July 2013.

[37] C. Bohler, P. Cheilaris, R. Klein, C. H. Liu, E. Papadopoulou, and M. Zavershynskyi. On the complexity of higher order abstract Voronoi diagrams. In *Proc. 40th International Colloquium on Automata, Languages and Programming (ICALP)*, volume 7965 of *LNCS*, pages 208–219, July 2013.

[38] E. Papadopoulou and M. Zavershynskyi. On higher-order Voronoi diagrams of line segments. In *Proc. 23rd International Symposium on Algorithms and Computation (ISAAC)*, volume 7676 of *LNCS*, pages 177–186, 2012.

[39] E. Papadopoulou and S. K. Dey. On the farthest line segment Voronoi diagram. In *Proc. 23rd International Symposium on Algorithms and Computation (ISAAC)*, volume 7676 of *LNCS*, pages 187–196, 2012.

[40] S. K. Dey and E. Papadopoulou. The L_∞ (L_1) farthest line segment Voronoi diagram. In *Proc. 9th International Symposium on Voronoi Diagrams in Science and Engineering (ISVD)*, pages 49–55. IEEE-CS, 2012.

[41] C.-H. Liu, E. Papadopoulou, and D. T. Lee. An output-sensitive approach for the L_1/L_∞ k-Nearest-Neighbor Voronoi diagram. In *Proc. 19th Annual European Symposium on Algorithms (ESA)*, volume 6942 of *LNCS*, pages 70–81, September 2011.

[42] E. Papadopoulou and J. Xu. The L_∞ Hausdorff Voronoi diagram revisited. In *Proc. Int. Symposium on Voronoi Diagrams in Science and Engineering (ISVD)*, pages 67–74. IEEE-CS, 2011.

[43] J. Xu, L. Xu, and E. Papadopoulou. Computing the map of geometric minimal cuts. In *Proc. 20th International Symposium on Algorithms and Computation*, volume 5878 of *LNCS*, pages 244–254, 2009.

[44] E. Papadopoulou. The higher order Hausdorff Voronoi diagram and VLSI critical area extraction for via-blocks. In *Proc. 5th Int. Symposium on Voronoi diagrams in Science and Engineering (ISVD)*, pages 181–191, 2008.

[45] E. Papadopoulou. Higher order Voronoi diagrams of segments for VLSI critical area extraction. In *Proc. 18th International Symposium on Algorithms and Computation (ISAAC)*, volume 4835 of *LNCS*, pages 716–727, 2007.

[46] M. Mukherjee, S. Mansfield, Z. Zhao, L. Liebmann, M. Lavin, A. Lvov, and E. Papadopoulou. The problem of optimal placement of sub-resolution assist features (SRAF). In *Proc. SPIE–Optical Microlithography XVIII*, volume 5754, pages 1417–1429, 2005.

[47] E. Papadopoulou. On the Hausdorff Voronoi diagram of point clusters in the plane. In *Proc. Workshop on Algorithms and Data Structures (WADS)*, number 2748 in Lecture Notes in Computer Science, pages 439–450, 2003.

[48] E. Papadopoulou and D. T. Lee. The min-max Voronoi diagram of polygonal objects and applications in VLSI manufacturing. In *Proc. 13th International Symposium on Algorithms and Computation*, number 2518 in Lecture Notes in Computer Science, pages 511–522, 2002.

[49] Z. Chen, E. Papadopoulou, and J.-H. Xu. Robustness of algorithm for k-gon metric Voronoi diagram construction. In *Proc. 14th Canadian Conference on Computational Geometry*, August 2002.

[50] E. Papadopoulou. Critical area computation for missing material defects in VLSI circuits. In *Proc. International Symposium on Physical Design*, pages 140–146, April 2000.

[51] E. Papadopoulou. l_∞ Voronoi diagrams and applications to VLSI layout and manufacturing. In *Proc. 9th International Symposium on Algorithms and Computation*, number 1533 in Lecture Notes in Computer Science, pages 9–18, 1998.

[52] E. Papadopoulou and D. T. Lee. Critical area computation – A new approach. In *Proc. International Symposium on Physical Design*, pages 89–94, 1998.

[53] O. Aichholzer, F. Aurenhammer, D. Chen, D. T. Lee, A. Mukhopadhya, and E. Papadopoulou. Voronoi diagrams for direction–sensitive distances. In *Proc. 13th Annual ACM Symposium on Computational Geometry*, pages 418–420, 1997.

[54] E. Papadopoulou. k-pairs non-crossing shortest paths in a simple polygon. In *Proc. 7th Annual International Symposium on Algorithms and Computation*, number 1178 in Lecture Notes in Computer Science, pages 305–314, December 1996.

[55] E. Papadopoulou and D. T. Lee. Efficient computation of the geodesic Voronoi diagram of points in a simple polygon. In *Proc. 3rd Annual European Symposium on Algorithms*, number 979 in Lecture Notes in Computer Science, pages 238–251, 1995.

[56] E. Papadopoulou and D. T. Lee. Shortest paths in a simple polygon in the presence of *forbidden* vertices. In *Proc. 6th Canadian Conference on Computational Geometry*, pages 110–115, August 1994.

Software – Peer Reviewed

[57] P. Cheilaris, S. K. Dey, and E. Papadopoulou. L_∞ segment Delaunay graph. Computational Geometry Algorithms Library (CGAL) `https://www.cgal.org`, in CGAL-4.7, 2015.

[58] Voronoi CAA: Voronoi Critical Area Analysis. IBM VLSI CAD Tool, Department of Electronic Design Automation, IBM Microelectronics Division, Burlington, VT. Distributed by Cadence. Patents: US6178539, US6317859, US7240306, US7752589, US7752580, US7143371, US20090125852.

Meetings with Published Abstracts

[59] K. Junginger and E. Papadopoulou. Deletion in abstract Voronoi diagrams in expected linear time. In *Abstracts 34th European Workshop on Computational Geometry (EuroCG)*, 2015.

[60] M. Claverol, E. Khramtcova, E. Papadopoulou, M. Saumell, and C. Seara. Stabbing circles for some sets of Delaunay segments in the plane. In *Abstracts 32nd European Workshop on Computational Geometry (EuroCG)*, 2016.

[61] E. Khramtcova and E. Papadopoulou. Randomized incremental construction for the Hausdorff Voronoi diagram. In *Abstracts of Computational Geometry: Young Researchers Forum (CG:YRF)*, 2015.

[62] M. Claverol, E. Khramtcova, E. Papadopoulou, M. Saumell, and C. Seara. Stabbing circles for sets of segments in the plane. In *Abstracts XVI Spanish Meeting on Computational Geometry (XVI EGC)*, 2015.

[63] E. Khramtcova and E. Papadopoulou. Linear-time algorithms for the farthest segment Voronoi diagram and related tree-structures. In *Abstracts 31st European Workshop on Computational Geometry (EuroCG)*, 2015.

[64] H. Bennett, E. Papadopoulou, and C. Yap. A subdivision approach to weighted Voronoi diagrams. In *Abstracts 24th Annual Fall Workshop on Computational Geometry*, 2014.

[65] G. Barequet and E. Papadopoulou. On farthest-site Voronoi diagrams of line segments and lines in three and higher dimensions. In *Abstracts 30th European Workshop on Computational Geometry (EuroCG)*, 2014.

[66] E. Khramtcova and E. Papadopoulou. A simple RIC for the Hausdorff Voronoi diagram of non-crossing clusters. In *Abstracts 30th European Workshop on Computational Geometry (EuroCG)*, 2014.

[67] P. Cheilaris, E. Khramtcova, and E. Papadopoulou. Randomized incremental construction of the Hausdorff Voronoi diagram of non-crossing clusters. In *Abstracts 29th European Workshop on Computational Geometry (EuroCG)*, pages 159–163, 2013.

[68] E. Papadopoulou and M. Zavershynskyi. A sweepline algorithm for higher-order Voronoi diagrams. In *Abstracts 29th European Workshop on Computational Geometry (EuroCG)*, pages 233–216, 2013.

[69] E. Papadopoulou and M. Zavershynskyi. On higher-order Voronoi diagrams of line segments. In *Abstracts 28th European Workshop on Computational Geometry (EuroCG)*, pages 233–236, 2012.

[70] E. Papadopoulou and S. K. Dey. On the farthest line segment Voronoi diagram. In *Abstracts 28th European Workshop on Computational Geometry (EuroCG)*, pages 237–240, 2012.

[71] E. Papadopoulou and J. Xu. The L_∞ Hausdorff Voronoi diagram revisited. In *Abstracts 27th European Workshop in Computational Geometry (EuroCG)*, pages 67–70, 2011.

[72] E. Papadopoulou. Geometric min-cuts, higher order Voronoi diagrams, and net-aware VLSI critical area extraction. In *Seventh Joint Operations Research Days*, Lugano, TI, Switzerland, September 2009.

[73] E. Papadopoulou. Higher order Voronoi diagrams of segments for VLSI critical area extraction. In *17th Fall Workshop on Computational and Combinatorial Geometry*, IBM T.J. Watson Research Center, Hawthorn, NY, U.S.A., 2007.

[74] E. Papadopoulou. Net-aware critical area extraction for VLSI opens via Voronoi diagrams. In *23rd European Workshop on Computational Geometry*, Graz University of Technology, Graz, Austria, March 2007.

[75] E. Papadopoulou. Voronoi diagrams for VLSI manufacturing: robustness and implementation. In *DIMACS Workshop on Implementations of Geometric Algorithms*, DIMACS Center, Rutgers University, Piscataway, NJ, U.S.A., December 2002.

[76] E. Papadopoulou and D. T. Lee. The L_∞ Voronoi diagram of segments and VLSI applications. In *Proc. of the 6th SIAM Conference on Geometric Design*, Albuquerque, NM, U.S.A., November 1999.

[77] E. Papadopoulou. VLSI critical area computation for missing material defects via L_∞ Voronoi diagrams. In *Proc. of the 8th Fall Workshop on Computational Geometry (FWCG)*, Johns Hopkins University, Baltimore, MD, U.S.A., October 1999.

[78] E. Papadopoulou and D. T. Lee. L_∞ Voronoi diagrams and applications in VLSI layout and manufacturing. In *Proc. of the 8th Fall Workshop on Computational Geometry (FWCG)*, Brown University, Providence, RI, U.S.A., October 1998.

Patents

[79] E. Papadopoulou. Method and apparatus for net-aware critical area extraction. Patent application US20090125852, May 2009.

[80] S. C. Braasch, J. Hibbeler, R. N. Kanj, D. Maynard, S. Nassif, and E. Papadopoulou. Method and system for analyzing an integrated circuit based on sample windows selected using an open deterministic sequencing technique. Patent US 7752580, July 2010.

[81] H. Xiang, E. Papadopoulou, R. Puri, and M. Y. Tan. Caa friendly global routing. Patent application US20080256502, October 2008.

[82] R. J. Allen, M. Guzowski, J. Hibbeler, D. Maynard, K. McCullen, E. Papadopoulou, S. Prue, and M. Y. Tan. A method, apparatus and computer program product for displaying and modifying the critical area of an integrated circuit design. Patent US7752589, July 2007.

[83] R. Gordon, A. Lvov, S. Mansfield, M. Mukherjee, and E. Papadopoulou. Optimized placement of subresolution assist features within two-dimensional environments. Patent application US20050202326, April 2005.

[84] R. J. Allen, P. Chan, E. Papadopoulou, S. Prue, and M.Y. Tan. A method to compute Critical Area with shapes biasing. Patent US7240306, July 2007.

[85] R. Allen, E. Papadopoulou, and M. Tan. Critical area computation of composite fault mechanisms using Voronoi diagrams. Patent US 7143371, January 2007.

[86] E. Papadopoulou and D. Maynard. IC design modeling allowing dimension-dependent rule checking. Patent US 7404164, July 2008.

[87] E. Papadopoulou. Method and system for determining Critical Area for missing material defects in circuit layouts. Patent US 6317859, November 2001.

[88] E. Papadopoulou and D. T. Lee. Method and system for determining Critical Area for circuit layouts. Patent US 6178539, January 2001.

[89] E. Papadopoulou, M. Lavin, G. Tellez, and A. Allen. An incremental method for Critical Area and Critical Region computation of via-blocks. Patent US6247853, June 2001.

[90] E. Papadopoulou and M. Lavin. Incremental Critical Area Computation for VLSI yield prediction. Patent US 6044208, April 2000.