Evanthia Papadopoulou

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RESEARCH INTERESTS

Design and Analysis of Algorithms
Computational Geometry and Applications
Algorithmic aspects of VLSI Computer-Aided Design – Manufacturability
Data Structures
Implementation of Algorithms

EDUCATION

Northwestern University, Department of EE/CS, Evanston, IL
Ph.D. in Computer Science, December 1995.
Thesis title: Path Optimization in Combined Metrics.
Advisor: Professor D.T. Lee. GPA: 4.0/4.0.

University of Illinois at Chicago, Chicago, IL
Master of Science in Computer Science, December, 1989. GPA: 4.92/5.0.

University of Athens, Department of Mathematics, Athens, Greece
Bachelor of Science in Mathematics, June, 1986.

PROFESSIONAL EXPERIENCE

Associate Professor, **Università della Svizzera italiana** (University of Lugano)
9/2008 – present Lugano, CH

IBM T.J. Watson Research Center, **Research Staff Member**, 4/98 – 2008 (on leave 10/2006–2008). **Postdoctoral Research Fellow**, 9/96 – 4/98
Yorktown Heights, NY

Research and development in *Computer-Aided Design* for VLSI Layout and Manufacturing based on concepts from *Discrete and Computational Geometry*. Introduced the L_∞ Voronoi diagram of VLSI layout shapes as a powerful tool to tackle a variety of deep submicron manufacturing related problems in VLSI design. A major project has been an integrated CAD tool, to predict the *yield* of VLSI chips in the presence of random manufacturing defects. This is an important problem in the semiconductor industry and has been addressed successfully by exploiting the geometric nature of VLSI designs based on mathematical concepts of generalized Voronoi diagrams. The resulting CAD tool is being widely used in production by IBM Microelectronics for the manufacturing of VLSI chips. The project resulted in a number of patents, publications, and has been highlighted in the "Innovation Matters" web page of IBM Research. For this work received the IBM Outstanding Innovation Award and a research rating of Technical Accomplishment. Funded jointly by IBM Research and IBM

Microelectronics.

Assistant Professor, **Athens University of Economics and Business**, Greece
while on sabbatical and leave of absence from IBM T.J. Watson Research Center
2004, 2006-2008.

Postdoctoral Researcher, **Northwestern University**, 1/1996–7/96, Evanston, IL
Research in Computational Geometry.

Visiting Researcher, **Academia Sinica**, Summer 1993, Taipei, Taiwan, R.O.C.
Research in geometric bi-criteria optimization problems with the group on Design and Analysis of Algorithms.

Research/Teaching Assistant, **Northwestern University**, 1990–1995, Evanston, IL

FUNDING

ESF/SNF project 20GG21-134355 – "Hausdorff and Higher-order Voronoi diagrams", 2011-2014. Funding: 295,050 CHF. Part of the collaborative European Science Foundation (ESF) research project EuroGIGA/VORONOI.

SNF project 200021-127137 – "Generalized Voronoi diagrams of polygonal objects: algorithms and applications", 2010-2013. Funding: 157'692 CHF.

AWARDS

- IBM Invention Achievement Award (Third Plateau), September 2007
- IBM Technical Accomplishment for "Voronoi diagram based Critical Area Analysis", December 2006.
- IBM Outstanding Innovation Award for "Voronoi diagram based Critical Area Analysis", August 2006
- IBM Invention Achievement Award (Second Plateau), March 2005
- IBM Research Division Award, for the "development and deployment of MASH", December 1999
- IBM Invention Achievement Award (First Plateau), July 1999
- IBM Invention Achievement Award (First Patent Application), May 1998
- Northwestern University annual Scholarships, 1990-1995 : full tuition and stipend.
- University of Illinois at Chicago annual Scholarships, 1988-1990: full tuition and stipend.

TEACHING and UNIVERSITY SERVICE

Università della Svizzera italiana (University of Lugano), 9/2008–Present, Lugano, CH

- Designed and taught the following undergraduate courses: Mathematical Foundations: Fall 2008, Discrete Mathematics I: Spring 2010, 2011, Fall 2011, Discrete Mathematics II: Spring 2009, Topics in Algorithms: Fall 2010.
- Designed and taught the following graduate courses: Computational Geometry-An Introduction: Spring 2009, Topics in Algorithms and Data Structures: Fall 2010, Introduction to Computational Geometry: Spring 2012.

- PhD student supervision: currently advising three PhD students at University of Lugano (two at their second year and one at her first year).
- PhD committee member for several PhD dissertations at University of Lugano, in progress (4), defended (3).
- Service: Exam Delegate & Director of Bachelor Program, Faculty of Informatics, since 2009.

Athens University of Economics and Business, Greece
- Undergraduate courses taught: Computer Graphics: Spring & Fall 2004, Data Structures: Fall 2006 & 2007, Automata and Complexity: Spring 2007 & 2008.
- Graduate courses taught: Automata and Complexity: Spring 2004, Graphics and Computational Geometry: Fall 2004, 2006 & 2007.
- Erasmus courses: Computational Geometry: Fall 2007.
- Academic coordinator of the Erasmus program, 2006-2008.

Northwestern University, 1991–1995, Evanston, IL
- **Instructor**. Taught course: EECS A20−Introduction to Computers and Information Technology. 1993–1995.
- **Teaching Assistant**. Assisted courses: Formal Languages and Automata, Design and Analysis of Algorithms, Data Structures, 1991 – 1993.

University of Illinois at Chicago, 1988–1990, Chicago, IL
- **Visiting Lecturer**. Taught course: Math191−Structured Programming with Pascal I. 1989-1990. Responsible for course planning, course organization, teaching and evaluating approximately 100 students.
- **Teaching Assistant**. Assisted courses: Structured Programming with Pascal I, Structured programming with Pascal II, Introduction to Calculus.

COMMUNITY SERVICE

- Hosted the kickoff meeting of the ESF project EuroGIGA/VORONOI at USI, Lugano, October 7-11, 2011.
- Program Committee member, ISVD 2010
- External Reviewer, Faculty grant proposals, University of Crete, Greece, 2011
- Have acted as a referee for the following international journals: Algorithmica, SIAM Journal on Computing, Computational Geometry: Theory and Applications, Computer Aided Geometric Design, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Information Processing Letters, International Journal of Computational Geometry and Applications, International Journal of Computer Mathematics, Networks, Wireless Communications and Mobile Computing.
- Have acted as a referee for the following international conferences at multiple years: ACM Symposium on Computational Geometry (SoCG), International Computing and Combinatorics Conference (COCOON), International Symposium on Algorithms and Computation (ISAAC), International Symposium on Voronoi diagrams in Science and Engineering (ISVD), EuroCG, Eurographics, IEEE Design Automation Conference (DAC).

SELECTED INVITED LECTURES

- Invited participant, workshop on "Computational Geometry and Applications", Bellairs Research Institute of McGill University, Holetown Barbados, January 2011.
- Lecture in Seminar Series: Optimization and Applications, Department of Computer Science, *ETH Zürich*, May 2010
- IBM-Research, Zürich, November 2009
- Faculty of Informatics, Karlsruhe Institute of Technology, October 2009
- Summer Research Institute (SuRI), *EPFL*, June 2009
- Seminar at IDSIA-Dalle Molle Institute for Artificial Intelligence, Lugano, March 2009
- Department of Computer Science. *ETH Zürich*, Zürich Switzerland, December 2008
- Faculty of Informatics. *University of Lugano*, Switzerland, February 2008, April 2007
- Department of Computer Science, University of Verona, Verona Italy, April 2008
- Department of Computer Science, University of Milan Biccoca, Milan, Italy, April 2007
- Tutorial at ICCAD 2006 – *International Conference on Computer Aided Design 2006*, "Random defect yield modeling and critical area computation", Part II of tutorial "DFM: Impact of manufacturing reality on design", C. Mack, D. Z. Pan, and E. Papadopoulou, San Jose, CA, Nov. 2006.
- Invited speaker/participant, "DIMACS Workshop on Implementation of Geometric Algorithms", DIMACS Center, Rutgers University, Piscataway NJ, December 4 - 6, 2002.
- Department of Informatics & Telecommunications, *University of Athens*, Athens, Greece, October 2002.
- Department of Electronic and Computer Engineering, Technical University of Crete, June 2002.
- Invited participant at the "Workshop on Pseudo Triangulations", Bellairs Research Institute of McGill University, Holetown Barbados, January 26-February 2, 2001.
- Department of Electrical and Computer Engineering, *University of Massachusetts*, Amherst, MA, October 2000.
- Invited speaker/participant at the minisymposium on *Voronoi Diagram and Medial Axis Computations* organized within the *6th SIAM Conference on Geometric Design*, Albuquerque, New Mexico, November 2-5, 1999.
- Department of Mathematics and Computer Science, *Universität Konstanz*,Germany, October 1999.
- Department of Electrical and Computer Engineering, *Sung Kyun Kwan University*, Suwon, Korea, December 1998.
- Department of Computer Science, *University of Ioannina*, Greece, September 1998.
- Department of Computer Science, *Stevens Institute of Technology*, Hoboken, New Jersey, March 1998.
- Invited lecturer/participant to the *Summer Institute on Computational Geometry and Applications*, Institute of Information Sciences, Academia Sinica, Taiwan, R.O.C, June 1996. The summer Institute consisted of one week of intensive lectures given by the invited participants and three weeks of research sessions on topics in Computational Geometry.

JOURNAL PUBLICATIONS

- J. Xu, L. Xu, and E. Papadopoulou, "Computing the Map of Geometric Minimal Cuts", Algorithmica, to appear.
- E. Papadopoulou, "Net-aware critical area extraction for opens in VLSI circuits via higher-order Voronoi diagrams", *IEEE Trans. on Comp.-Aided Design*, 30(5), pp. 704-716, 2011.
- Zhenming Chen, Evanthia Papadopoulou, Jinhui Xu, "Robustness of k-gon Voronoi diagram construction", *Information Processing Letters*, Vol. 97, no 4, 2006, 138-145.
- Evanthia Papadopoulou and D.T. Lee, "The Hausdorff Voronoi diagram of polygonal objects: a divide and conquer approach", *International Journal of Computational Geometry and Applications*, Vol. 14, No. 6, December 2004, 421-452.
- Evanthia Papadopoulou, "The Hausdorff Voronoi diagram of point clusters in the plane", *Algorithmica*, 40, 2004, 63-82.
- Evanthia Papadopoulou, "Critical Area computation for missing material defects in VLSI circuits", *IEEE Transactions on Computer-Aided Design*, vol. 20, no.5, May 2001, 583-597.
- E. Papadopoulou and D.T. Lee, "The L_∞ Voronoi diagram of segments and VLSI applications", *International Journal of Computational Geometry and Applications*, Vol. 11, No. 5, 2001, 503-528.
- Evanthia Papadopoulou, "k-Pairs non-crossing shortest paths in a simple polygon", *International Journal of Computational Geometry and Applications*, vol. 9. No. 6, December 1999, 533-552.
- E. Papadopoulou and D.T. Lee, "Critical Area computation via Voronoi diagrams", *IEEE Transactions on Computer-Aided Design*, vol. 18, No. 4, April 1999, 463-474.
- O. Aichholzer, F. Aurenhammer, D. Chen, D.T. Lee and E. Papadopoulou, "Skew Voronoi diagrams", *International Journal of Computational Geometry and Applications*, Vol. 9, No. 3, June 1999, 235-248.
- E. Papadopoulou and D.T. Lee, "A new approach for the geodesic Voronoi diagram of points in a simple polygon and other restricted polygonal domains", *Algorithmica*, Vol. 20, No. 4, April 1998, 319-352.
- E. Papadopoulou and D.T. Lee, "The all-pairs quickest path problem", *Information Processing Letters*, April 1993, 45, 261-267.

JOURNAL SUBMISSIONS - UNDER REVIEW

- E. Papadopoulou and J. Xu. The L_∞ Hausdorff Voronoi diagram revisited. Submitted to *Computational Geometry: Theory and Applications.*

BOOK CHAPTERS

- E. Papadopoulou, J. Xu, and L. Xu. Map of Geometric Minimal Cuts with Applications. Book chapter in *Handbook of Combinatorial Optimization*, 2nd Edition, 2013, Pardalos, Panos M.; Du, Ding-Zhu; Graham, Ronald (Eds.), Springer.

- Puneet Gupta and Evanthia Papadopoulou, "Yield Analysis and Optimization", Chapter 7.3 in C.J. Alpert, D.P. Mehta, S.S. Sapatnekar editors, "The Handbook of Algorithms for VLSI Physical Design Automation", Taylor & Francis CRC Press, November 2008.

PUBLICATIONS IN CONFERENCE PROCEEDINGS

- Chih-Hung Liu, Evanthia Papadopoulou, and D. T. Lee. An Output-Sensitive Approach for the L_1/L_∞ k-Nearest-Neighbor Voronoi Diagram, *Proc. 19th Annual European Symposium on Algorithms*, ESA 2011, LNCS 6942, 70-81.

- E. Papadopoulou and J. Xu, "The L_∞ Hausdorff Voronoi diagram revisited", *Proc. 8th Int. Symposium on Voronoi Diagrams in Science and Engineering*, ISVD 2011, IEEE-CS, 67-74.

- J. Xu, L. Xu, and E. Papadopoulou, "Computing the Map of Geometric Minimal Cuts", *Proc. 20th International Symposium on Algorithms and Computation, ISAAC 2009*, LNCS 5878, 244-254.

- E. Papadopoulou, "The higher order Hausdorff Voronoi diagram and VLSI critical area extraction for via-blocks", *Proc. 5th International Symposium on Voronoi Diagrams in Science and Engineering*, September 2008, Kyiv Ukraine, 181-191.

- E. Papadopoulou, "Higher order Voronoi diagrams of segments for VLSI critical area extraction", *Proc. 18th International Symposium on Algorithms and Computation*, December 2007, Sendai, Japan, *Lecture Notes in Computer Science 4835*, 716-727.

- M. Mukherjee, S. Mansfield, Z. Zhao, L. Liebmann, M. Lavin, A. Lvov, E. Papadopoulou, "The problem of optimal placement of sub-resolution assist features (SRAFs)", *Proc. SPIE–Optical Microlithography XVIII*, SPIE'05, vol.5754, 1417-1429.

- E. Papadopoulou, "On the Hausdorff Voronoi diagram of point clusters in the plane", *Proc. Workshop on Algorithms and Data Structures*, WADS 2003, Ottawa, Canada, *Lecture Notes in Computer Science 2748*, 439-450.

- E. Papadopoulou and D.T. Lee, "The min-max Voronoi diagram of polygonal objects and applications in VLSI manufacturing", *Proc. 13th International Symposium on Algorithms and Computation*, November 2002, Vancouver, Canada, *Lecture Notes in Computer Science 2518*, 511-522.

- Z. Chen, E. Papadopoulou, and J. H. Xu, "Robustness of algorithm for k-gon metric Voronoi diagram construction", *Proc. 14th Canadian Conference on Computational Geometry*, University of Lethbridge, Lethbridge, Canada, August 2002.

- Evanthia Papadopoulou, "Critical area computation for missing material defects in VLSI

circuits", *Proc. International Symposium on Physical Design*, San Diego, CA, April 2000, 140-146.

- Evanthia Papadopoulou, "L_∞ Voronoi diagrams and applications to VLSI layout and manufacturing", *Proc. 9th International Symposium on Algorithms and Computation*, December 1998, Taejon, Korea, *Lecture Notes in Computer Science 1533*, 9-18.

- E. Papadopoulou and D.T. Lee, "Critical area computation – A new approach", Proc. *International Symposium on Physical Design*, Monterey, CA, April 1998, 89-94.

- Evanthia Papadopoulou, "k-Pairs non-crossing shortest paths in a simple polygon", *Proc. 7th Annual International Symposium on Algorithms and Computation*, December 1996, *Lecture Notes in Computer Science 1178*, 305-314.

- O. Aichholzer, F. Aurenhammer, D. Chen, and D.T. Lee, A. Mukhopadhyay, and E. Papadopoulou, "Voronoi diagrams for direction–sensitive distances", Proc. *13th Annual ACM Symposium on Computational Geometry*, Nice, France 1997, 418-420

- E. Papadopoulou and D.T. Lee, "Efficient computation of the geodesic Voronoi diagram of points in a simple polygon", *Proc. 3rd Annual European Symposium on Algorithms*, September 1995. *Lecture Notes in Computer Science 979*, pp. 238-251.

- E. Papadopoulou and D.T. Lee, "Shortest paths in a simple polygon in the presence of *forbidden* vertices", *Proc. 6th Canadian Conference on Computational Geometry*, August 1994, pp. 110-115.

ADDITIONAL CONFERENCE ABSTRACTS

- E. Papadopoulou and J. Xu, "The L_∞ Hausdorff Voronoi diagram revisited", *27th European Workshop in Computational Geometry*, EuroCG 2011, Morschach, Switzerland, March 2011.

- E. Papadopoulou, "Geometric min-cuts, higher order Voronoi diagrams, and net-aware VLSI critical area extraction", Seventh Joint Operations Research Days, Ticino, Switzerland, September 2009.

- E. Papadopoulou, "Higher order Voronoi diagrams of segments for VLSI critical area extraction", 17th Fall workshop on Computational and Combinatorial Geometry, IBM T.J. Watson Research Center, Hawthorn NY, November 2007.

- E. Papadopoulou, "Net-aware critical area extraction for VLSI opens via Voronoi diagrams", 23rd European Workshop on Computational Geometry, Graz University of Technology, Austria, March 2007.

- E. Papadopoulou, "Voronoi diagrams for VLSI manufacturing: robustness and implementation", DIMACS Workshop on Implementations of Geometric Algorithms, DIMACS Center, Rutgers University, Piscataway, NJ, Dec. 2002

- E. Papadopoulou and D.T. Lee, "The min-max Voronoi diagram of polygonal objects and applications in VLSI manufacturing", *DIMACS Workshop on Computational Geometry*,

DIMACS Center, Rutgers University, Piscataway, NJ, November 2002.

- E. Papadopoulou and D.T. Lee, "The L_∞ Voronoi diagram of segments and VLSI applications", *6th SIAM Conference on Geometric Design*, Albuquerque, New Mexico, November 2-5, 1999.

- Evanthia Papadopoulou,"VLSI critical area computation for missing material defects via L_∞ Voronoi diagrams", *4th CGC Workshop on Computational Geometry*, Johns Hopkins University, Baltimore, MD, October 15-16, 1999.

- Evanthia Papadopoulou and D.T. Lee, "L_∞ Voronoi diagrams and applications in VLSI layout and manufacturing", *3rd CGC Workshop on Computational Geometry*, Brown University, Providence, RI, October 11-12, 1998.

CONFERENCE ABSTRACT SUBMISSIONS - UNDER REVIEW

- E. Papadopoulou and S. K. Dey, "On the farthest line-segment Voronoi diagram", submitted to EuroCG 2012.
- E. Papadopoulou and M. Zavershynskyi "On the higher-order line segment Voronoi diagram", submitted to EuroCG 2012.

OTHER PUBLICATIONS

- "VLSI Critical Area Analysis via Voronoi Diagrams", article in the *Innovation Matters* web page of IBM Research, March 2006.
http://domino.research.ibm.com/comm/research.nsf/pages/d.ee.html.

PATENTS FILED WITH U.S PATENT AND TRADEMARK OFFICE

- "Method and apparatus for net-aware critical area extraction", E. Papadopoulou, Patent application US20090125852, Filled November 2007
- "Method and system for analyzing an integrated circuit based on sample windows selected using an open deterministic sequencing technique", S. C. Braasch, J. Hibbeler, R. N Kanj, D. Maynard, S. Nassif, E. Papadopoulou, Patent application US20090031263, Filed April 2007
- "Method and apparatus for net-aware critical area extraction", E. Papadopoulou, S.C. Braasch, M.Y. Tan, YOR920060300US1, Filed January 2007.
- "CAA friendly global routing", Hua Xiang, E. Papadopoulou, R. Puri, M.Y. Tan, Patent Application US20080256502, Filed April 2007
- "A method, apparatus and computer program product for displaying and modifying the critical area of an integrated circuit design", R.J. Allen, M. Guzowski, J. Hibbeler, D. Maynard, K. McCullen, E. Papadopoulou, S. Prue, M.Y. Tan, Patent application US20080168414, Filed December 2006.
- "Optimized placement of subresolution assist features within two-dimensional environments", R. Gordon, A. Lvov, S. Mansfield, M. Mukherjee, E. Papadopoulou, Patent application US20050202326, Filed April 2004.
- "A method to compute Critical Area with shapes biasing", R.J. Allen, P. Chan, E. Papadopoulou, S. Prue, M.Y. Tan, US7240306, issued July 2007
- "Critical Area computation of composite fault mechanisms using Voronoi diagrams", R. Allen, E. Papadopoulou, M. Tan, US 7,143,371, issued January 2007.
- "IC design modeling allowing dimension-dependent rule checking", E. Papadopoulou and D. Maynard, US 7404164, issued July 2008.
- "Method and system for determining Critical Area for missing material defects in circuit layouts", E. Papadopoulou, US 6317859, issued November 2001.
- "Method and system for determining Critical Area for circuit layouts", E. Papadopoulou and D.T. Lee, US 6178539, issued January 2001.
- "An incremental method for Critical Area and Critical Region computation of via-blocks" E. Papadopoulou, M. Lavin, G. Tellez, and A. Allen, US6247853, issued June 2001.
- Incremental Critical Area Computation for VLSI Yield Prediction", E. Papadopoulou and M. Lavin, US 6044208, issued April 2000.